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<div style="position: absolute; left: -50px; top: 50px; border: 1px solid black; border-radius: 50%; padding: 5px; transform: rotate(-45deg); font-size: 8px;"> APR 23 2004 U.S. PATENT & TRADEMARK OFFICE </div>				Application Number 10/758,977	
				Filing Date January 14, 2004	
				First Named Inventor: Kenneth S. McElvain	
				Art Unit Not Yet Assigned 2825	
				Examiner Name Not Yet Assigned LIN, SUN J.	
Sheet 1 of 1				Attorney Docket Number 002986.P045	
NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²		
JSL		LYONS et al., "The Use of Triple-Modular Redundancy to Improve Computer Reliability," IBM Journal, April 1962, pp. 200-209.			
		HABINC, "Functional Triple Modular Redundancy (FTMR)" Gaisler Research, Version 0.2, December 2002, 56 pgs.			
		FRANCO, et al., "FPGA Implementation of a Serial Organized DA Multichannel FIR Filter," Tenth ACM International Symposium on Field Programmable Gate Arrays, Monterey, California, February 24-26, 2002.			
		HALPERIN, et al., "Combinatorial Approximation Algorithms for the Maximum Directed Cut Problem," Proceedings of 12 th Symposium on Discrete Algorithms, pp. 1-7, 2001.			
		PARHI, Keshab K., "VLSI digital signal processing systems: design and implementation," Wiley-Interscience, pp. 91-118 & 149-187, 1999.			
JSL		THORNTON, James E., "Parallel Operation in the Control Data 6600," AFIPS Proc. FJCC, pt. 2, vol. 26, pp. 33-40, 1964.			

Examiner Signature		Date Considered	5-25-06
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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/758,977
				Filing Date	01/14/2004
				First Named Inventor:	McElvain
				Art Unit	2810 2825
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		WEAVER, NICHOLAS; MARKOVSKIY, YURY; PATEL, YATISH; WAWRZYNEK, JOHN; "Post-Placement C-Slow Retiming for the Xilinx Virtex FPGA" 10 pages. Copyright 2003 ACM 1-58113-651 - X/03/0002 FPGA '03, February 23 - 25, Monterey, California USA.			
		NOTIFICATION TO PAY ADDITIONAL FEES for International Application No. PCT/US2004/010006 (Attorney Docket No. 2986.P031PCT), mailed 06/23/2005, 8 pages. European Patent Office, Rijswijk. Authorized Officer: Iveta Bujanska			
		SHALASH, Ahmad F., et al., "Power Efficient Fir Folding Transformation For Wireline Digital Communications", Copyright 1998 IEEE, 0-7803-5148-7/98, pages 1816-1820.			
		SUNDARARAJAN, Vijay, et al., "Synthesis of Low Power Folded Programmable Coefficient Fir Digital Filters", Copyright 2000, IEEE, 0-7803-5973-9/00, pages 153-156.			
		LIN, John, et al., "A New Multi-Algorithm Multichannel Cascadable Digital Filter Processor", IEEE 1988 Custom Integrated Circuits Conference, CH2584-1/88/0000-0060. Copyright 1988 IEEE. Pages 10.7.1 - 10.7.5.			
		HASSOUN, Soha, et al., "Architectural Retiming: Pipelining Latency-Constrained Circuits" Copyright 1996 ACM, Inc. 0-89791-833-9/96/0006, pages 708-713. 33 rd Design Automation Conference. XP-002330653			
		PARHI, Keshab K., et al., "Synthesis of Control Circuits in Folded Pipeline DSP Architectures", Copyright 1992 IEEE, 0018-9200/92503.00 Vol. 27, No. 1, January 1992. pages 29 - 43.			

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